

In re the Application of: FURUHATA et al.

Serial No.: 09/599,477

Filed: June 23, 2000

For: SEMICONDUCTOR DEVICES
INCLUDING A NON-VOLATILE
MEMORY TRANSISTOR

Group Art Unit: 2826

Examiner: Dickey, T.

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TECHNOLOGY CENTER 2300ASSISTANT COMMISSIONER OF PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

☐ Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified statement previously submitted.☐ A verified statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.☐ No additional fee is required.

The fee has been calculated as shown below:

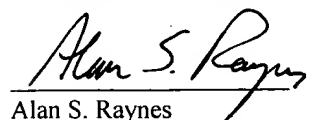
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO PREVIOUSLY PAID FOR		PRESENT EXTRA RATE		ADDIT. FEE	OR	RATE	ADDIT. FEE
TOTAL	34	MINUS	32	=	2	x	\$0	OR	x 18	\$36
INDEP CLAIMS *	5	MINUS	3	=	2	x	\$0	OR	x 84	\$168
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEP. CLAIM						+	\$	OR	+ 280	\$0
					TOTAL		\$0	OR	TOTAL	\$204

☐ Please charge Deposit Account No. 50-0585 the amount of \$___ to cover the extension fee and also the amount of \$___ to cover the claim fee. A duplicate copy of this sheet is enclosed.

- ☒ A check in the amount of \$ 920 to cover the extension fee is enclosed.
- ☒ A check in the amount of \$ 204 to cover the filing fee for additional claims is enclosed.
- ☐ A check in the amount of \$ _____ to cover the petition fee is enclosed.
- ☐ A check in the amount of \$ _____ to cover the Information Disclosure Statement fee is enclosed.

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. No. 50-0585. A duplicate of this sheet is enclosed.☒ Any filing fees under 37 CFR 1.16 for the presentation of extra claims.☒ Any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,



Alan S. Raynes

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315 South Beverly Drive, Suite 210

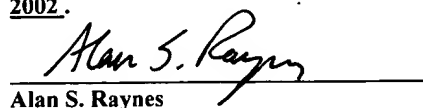
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Dated: March 25, 2002

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on March 25, 2002.
Alan S. RaynesMarch 25, 2002
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



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AMENDMENT

Assistant Commissioner for Patents
 Washington, D.C. 20231

Dear Sirs:

In response to the Office Action dated September 25, 2002, the time for response being extended to March 25, 2002 by the enclosed petition for extension of time, please enter and consider the following:

IN THE TITLE:

Please delete the title and insert the following:

--Semiconductor Devices Including a Multi-Well and Split-Gate Non-Volatile Memory
 Transistor Structure --

IN THE CLAIMS:

Please amend claims 1, 4, 6, 9, 15, 22, and 24-27 as follows:

1. (amended) A semiconductor device having a non-volatile memory transistor having a split-gate structure, the semiconductor device comprising:
- a semiconductor substrate of a first conductivity type having a memory region;
 - a first well of a second conductivity type located in the memory region; and
 - a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well.